REMARKS

The Office Action mailed January 16, 2003, has been received and reviewed. Claims 1-97 are currently pending in the application. Claims 36-75 and 87-97 have been withdrawn from consideration and cancelled without prejudice or disclaimer. The election to prosecute claims 1-35 and 76-86 is hereby acknowledged without any further traverse. Claims 1-24, 29-35 and 76-86 stand rejected. Claims 25-28 have been objected to as being dependent upon rejected base claims, but the indication of allowable subject matter in such claims is noted with appreciation. Reconsideration is respectfully requested.

Drawings

Applicant submits herewith, under cover of a separate Letter to the Official Draftsperson, proposed corrections to FIGS. 2, 6-8, 10, 11 and 14 of the drawings. Specifically, FIG. 2 was corrected to include reference numeral 74 and its corresponding lead line. FIGs. 6, 7 and 8 were designated "prior art" as suggested by the Examiner. FIG. 6 was also corrected to include reference numeral 724. FIG. 10 was corrected to include reference numeral 974 . FIG. 11 has been corrected to include reference numeral 1030 and its corresponding lead line. FIG. 14 is corrected to include reference numeral 930 and its accompanying lead line.

Further, applicant submits that the specification includes a description of reference signs 921 (paragraph 44), 924 (paragraph 48) and 926 (paragraph 42).

Applicant respectfully disagrees with the rejection of the drawings fail to show the combination of claims 22 and 23, 22-24 or claims 76-78. Claim 22 is at least depicted in FIGs. 9, 11 and 14. Claim 23 further requires at least one additional semiconductor die between the first and second semiconductor die. FIGs. 5 and 13 depict embodiments of the invention with more than two semiconductor die. Claim 24 further recites the at least one additional semiconductor die and the first semiconductor die are electrically connected. Applicants respectfully submit that one skilled in the art would understand the elements of claims 23 and 24 when viewing all of the figures together with the description in the specification. Reconsideration and withdrawal of the objection is requested.

Applicant respectfully submits that FIG. 3, together with the description in the specification, shows the combination of claims 76 and 77 and 76-78. Specifically, in paragraphs 35 and 36, it is discussed that a plurality of bond pads 32 are connected to the integrated circuitry of the semiconductor. Redistribution bond pads 36, 38 are independent from the integrated circuitry. Applicant submits that bond pads connected to integrated circuitry are known in the art. Further, FIG. 4 and the specification describe the formation of conductive traces connecting the first redistribution bond pad 36 to a second redistribution bond pad 38. (Specification, paragraphs 37 and 38). Reconsideration and withdrawal of the objection is requested.

All proposed corrections have been marked in red. Applicants respectfully request approval of the corrections to the drawings.

35 U.S.C. § 102(b)

Anticipation Rejection Based on Japanese Patent 6-132474 to Yamada et al.

Claims 1-3, 5-24, 21 [sic], 32-35, and 76-86 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamada et al., Japanese Patent 6-132474. Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Yamada discloses high density mounting for a semiconductor device. A first semiconductor 5c is mounted above a wiring substrate 3 with bump electrodes 6c such that the active region 7c of the first semiconductor die 5c faces the wiring substrate 3a. A second semiconductor 5b is positioned between the first semiconductor 5c and the wiring substrate 3, such that the active region 7b of the second semiconductor 5b faces the active region 7c of the first semiconductor 5c, and is electrically connected to the active region 7c of the first semiconductor 5c with bump electrodes 6b. A third semiconductor 5a is positioned between the first semiconductor 5c and the second semiconductor 5b, such that the active region 7a of the third

semiconductor 5a faces the active region 7b of the second semiconductor 5c, and is electrically connected to the active region 7b of the second semiconductor 5b with bump electrodes 6a. (Yamada, FIG. 1).

FIGs. 2(a) through 2(j) of Yamada depict a semiconductor 5b with a redistribution layer that facilitates electrical communication between the integrated circuitry thereof and that of another semiconductor 5a, as well as with integrated circuitry of yet another semiconductor 5c. In particular, semiconductor 5b includes a first bond pad 8b that is electrically connected to a second bond pad 10a in a vertical fashion, as well as a third bond pad 11a that communicates with the second bond pad 10a by way of a circuit trace. (Yamada, FIGs. 2(a)-2(c)). As shown in FIG. 2(j), a bump electrode 6b protrudes from the first bond pad 8b of the semiconductor 5b to electrically connect the same to a corresponding bond pad of semiconductor 5c, while another bump electrode 6a electrically connects the third bond pad 11a of semiconductor 5b and, thus, the same integrated circuit with which first bond pad 8b communicates, to a corresponding bond pad of the third semiconductor 5a.

Applicant respectfully submits that Yamada fails to disclose, either inherently or expressly, every element of the presently claimed invention. Independent claims 1 and 76 of the presently claimed invention, as amended and presented herein, include recitations of similar elements of at least one redistribution bond pad circuit "electrically isolated from" the integrated circuitry of the semiconductor die. Applicant submits that all of the bond pads in Yamada appear to be electrically connected to the integrated circuitry of the various semiconductors. As shown in FIG. 2(c) in Yamada, the bond pad 8(b)(8a, 8c) is electrically connected to a second bond pad 10(a) which is electrically connected to a third bond pad 11a (11b). At least the third bond pad 11a is within the active region 7b and thus connected to the integrated circuitry of the semiconductor. (Compare Yamada FIG. 1, FIG. 2(c) and FIG. 2(j)). As the three identified bond pads (8(a,b,c), 10(a,b,c) and 11(a,b,c)) are all connected, applicant respectfully submits that Yamada fails to disclose, either expressly or inherently, a redistribution bond pad circuit independent from the integrated circuitry of the semiconductor. Accordingly independent claims 1 and 76 of the presently claimed invention are not anticipated by Yamada and are allowable.

Claims 2 through 21 are each allowable as depending, either directly or indirectly, from

allowable claim 1.

Claim 7 is further allowable as Yamada fails to disclose, either expressly or inherently, the peripheral edges of said first semiconductor die and edges of said second semiconductor die are substantially vertically aligned. Instead, Yamada teaches each of the semiconductors have different sizes to allow bump electrodes (6a,b,c) to electrically connect the semiconductors.

Claim 18 is further allowable as Yamada fails to disclose, either expressly or inherently, that the at least one electrical connector comprises a solder ball.

Claims 77 through 86 are each allowable as depending, either directly or indirectly, from allowable claim 76.

Independent claim 22 of the presently claimed invention, as amended and presented herein, recites a "semiconductor assembly, comprising: a substrate; a first semiconductor die including an active surface, a second surface, and a plurality of peripheral edges, said second surface disposed on said substrate, said active surface having a plurality of bond pads thereon; a second semiconductor die including an active surface, a second surface, a plurality of peripheral edges and a plurality of bond pads on said active surface, said active surface of said second semiconductor die facing said active surface of said first semiconductor die, at least one bond pad of said plurality of bond pads of said first semiconductor die communicating with a corresponding redistribution circuit of said second semiconductor die, said redistribution circuit being electrically isolated from integrated circuitry of said second semiconductor die, at least one edge of said plurality of peripheral edges of said second semiconductor die extending laterally beyond at least one corresponding peripheral edge of said plurality of peripheral edges of said first semiconductor die; and at least one connective element extending from at least one bond pad of said plurality of bond pads on said active surface of said second semiconductor die to a corresponding contact area of said substrate adjacent to said at least one corresponding peripheral edge of said first semiconductor die."

Applicant respectfully submits that Yamada fails to disclose, either expressly or inherently, every element of independent claim 22. Specifically, Yamada fails to disclose, either expressly or inherently, a second semiconductor die which includes at least one redistribution circuit that is electrically isolated from integrated circuitry of the second semiconductor die. Instead, all of the

redistribution circuits that are described in Yamada communicate with integrated circuitry of the semiconductor dice described therein. As Yamada fails to disclose every element of the presently claimed invention, applicants submit that Yamada fails to anticipate claim 22. Accordingly, claim 22 of the presently claimed invention is allowable.

Claims 23 through 35 are each allowable as depending, either directly or indirectly from allowable claim 22.

35 U.S.C. § 103(a)

Obviousness Rejection Based on Japanese Patent 6-132474 to Yamada et al.

Claims 4, 29 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamada et al. (Japanese Patent 6-132474) as applied to claims 1, 3, 22, and 24 above, and further in view of Nguyen et al. (U.S. Patent 6,238,949). Applicant respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claims 4, 29 and 32 obvious, cannot serve as a basis for rejection.

Objections to Claims 25-28/Allowable Subject Matter

Claims 25-28 stand objected to as being dependent upon rejected base claims, but are indicated to contain allowable subject matter and would be allowable if placed in appropriate independent form. Applicants respectfully submit that claims 25 through 28 are allowable for the reasons set forth herein. Additionally, applicants submit new claims 98 through 108 for consideration. New claim 98 is claim 25 rewritten in independent form. Claims 99 through 108 are substantially similar to dependent claims 26 through 35. Thus, applicants submit no new matter is added in claims 98-108 and the claims are allowable.

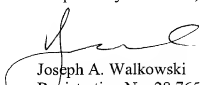
ENTRY OF AMENDMENTS

The amendments to the claims above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 35, 76 through 86 and 97 through 108 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



Joseph A. Walkowski
Registration No. 28,765
Attorney for Applicant
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: April 16, 2003
JAW/jml:djp

Document in ProLaw